ABSTRACT OF THE DISCLOSURE

A clock layout method comprises accepting circuit information on a logic circuit, placing a route driver on a semiconductor chip and forming initial clock routing with an H-tree structure in a local area and with a star structure in a global area, specifying a second node which first appears on a first wire among a plurality of wires branching from an arbitrary first node in the initial clock routing, specifying at least a third node which is the second to appear on a wire other than the first wire among the plurality of wires branching from the first node, defining the defined third node which exists in a direction within a predetermined angle from an input direction of a signal inputted to the second node, among the third nodes, folding a wire from the first node up to the defined third node and a node present therebetween.